What is claimed is:

1. A cell structure of non-volatile memory device using a nitride layer as a floating gate spacer comprising:

a gate stack including,

a first portion of a floating gate formed over a semiconductor substrate,

a control gate formed over at least part of the first portion of the floating gate, and

an exposed non-nitride spacer adjacent to sidewalls of the first portion of the floating gate; and

a floating gate transistor including,

a second portion of the floating gate formed over the semiconductor substrate to substantially overlap a portion of at least one of a source and drain implanted in the semiconductor substrate.

2. The cell structure of claim 1, wherein the gate stack further includes,

an insulating pattern including a nitride layer between the control gate and the first portion of the floating gate.

3. The cell structure of claim 1, wherein the floating gate transistor further includes,

a nitride spacer adjacent to sidewalls of the second portion of the floating gate

4. The cell structure of claim 1, wherein the non-nitride spacer includes a polysilicon layer and an oxide layer.

5. The cell structure of claim 1, further comprising:

a nitride spacer adjacent to sidewalls of the control gate.

6. The cell structure of claim 1, wherein the first and second portions of the floating gate comprise a polysilicon doped with impurity ions.

7. The cell structure of claim 1, further comprising:

an insulating pattern of the gate stack formed between the second portion of the floating gate and the semiconductor substrate, the insulating pattern including at least one of an oxide-nitride-oxide (ONO) layer and a nitride-oxide (NO) layer.

8. The structure of claim 1, wherein the control gate includes a polysilicon layer doped with impurity ions and a silicide layer, and a silicide layer is formed on the source and drain.

9. The cell structure of claim 1, wherein the non-volatile memory device is at least one of an erasable programmable read-only memory device (EPROM) and a flash memory device.

10. The cell structure of claim 1, wherein the at least one of an implanted source and drain is operable to inject charges into the first portion of the floating gate in response to a first voltage being applied to the control gate and a second voltage being applied to the second portion of the floating gate, thereby programming a corresponding cell of the non-volatile memory device.

11. The cell structure of claim 8, wherein the first portion of the floating gate is operable to discharge the injected charges to the at least one of an implanted source and drain in response to ultraviolet rays being applied to the exposed non-nitride spacer of the gate stack, thereby erasing the programmed cell.

12. A method for fabricating a cell structure of a non-volatile memory device, the method comprising:

forming a floating gate over a semiconductor substrate, a first portion of the floating gate being formed over a gate stack region of the semiconductor substrate, and a second portion of the floating gate being formed over a floating gate transistor region of the semiconductor substrate;

forming a control gate over at least a part of the first portion of the floating gate; and

forming a non-nitride spacer adjacent to sidewalls of the first portion of the floating gate.

13. The method of claim 12, further comprising:

implanting impurity ions into the semiconductor substrate to implant a source and drain at least partially in the floating gate transistor region of the semiconductor substrate, wherein the second portion of the floating gate substantially overlaps a portion of at least one of the implanted source and drain.

14. The method of claim 13, further comprising:

forming a nitride spacer over the floating gate transistor region, the formed nitride spacer being adjacent to sidewalls of the second portion of the floating gate; and

forming a silicide layer over the control gate, and over portions of the source and drain over which neither the second portion of the floating gate, nor the nitride spacer, is formed.

15. The method of claim 12, wherein the step of forming the non-nitride spacer includes,

forming a polysilicon spacer over the gate stack region, the formed polysilicon spacer being adjacent to sidewalls of the first portion of the floating gate, and

forming an oxide spacer over the formed polysilicon spacer.

16. The method of claim 12, wherein a nitride spacer is formed over the first portion of the floating gate, the formed nitride spacer being adjacent to sidewalls of the control gate.

17. The method of claim 12, wherein the step of forming the floating gate includes forming a polysilicon doped with impurity ions over the gate stack and floating gate transistor regions.

18. The method of claim 12, further comprising:

forming an insulating pattern over the gate stack region, the insulating pattern including at least one of an oxide-nitride-oxide (ONO) layer and a nitride-oxide (NO) layer.

19. The method of claim 12, wherein the step of forming the control gate includes forming a polysilicon doped with impurity ions and a silicide layer over the first portion of the floating gate.

20. The method of claim 12, wherein the step of forming the floating gate includes,

forming a field insulating pattern over the gate stack region;

forming a gate insulating pattern over the floating gate transistor region;

forming a polysilicon pattern over the gate stack region and the floating gate transistor region, the first portion of the floating gate comprising a part of the polysilicon pattern formed over the gate stack region, the second portion of the floating gate comprising a part of the polysilicon pattern formed over the floating gate transistor region.

21. The method of claim 20, further comprising:

etching at least the first portion of the floating gate to expose a surface area of the field insulating layer.

22. The method of claim 21, further comprising:

forming an insulating pattern including a nitride layer over the first and second portions of the floating gate.

23. The method of claim 21, further comprising:

forming a polysilicon layer doped with impurity ions over the first portion of the floating gate and the exposed surface area of the field insulating layer; and

etching the formed polysilicon layer to form the control gate over the first portion of the floating gate.

24. The method of claim 23, wherein:

the step of etching the formed polysilicon layer forms a polysilicon spacer over the exposed surface area of the field insulating layer, the polysilicon spacer being adjacent to sidewalls of the first portion of the floating gate, and

the step of forming the non-nitride spacer includes oxidizing the polysilicon spacer.

25. A non-volatile memory whose cell structure is manufactured according to the method of claim 12.

26. A non-volatile memory including:

a floating gate formed over a semiconductor substrate;

a non-nitride spacer adjacent to a first portion of the floating gate; and

a nitride spacer adjacent to a second portion of the floating gate, the second portion substantially overlapping at least one of a source and drain in the semiconductor substrate.

27. The non-volatile memory of claim 26, further comprising:

a control gate formed over the first portion of the floating gate.

28. The non-volatile memory of claim 27, wherein the at least one of the source and drain is operable to inject charges into the floating gate via hot carrier injection, thereby programming a cell in the non-volatile memory.

29. The non-volatile memory of claim 28, wherein

the control gate is operable to receive a first voltage;

at least one of the source, drain, and second portion of the floating gate is operable to receive a second voltage; and

the receiving of the first and second voltages causes the at least one of the source and drain to inject the charges via hot carrier injection.

30. The non-volatile memory, wherein the first portion of the floating gate is operable to discharge charges in response to ultraviolet rays being applied to at least a portion of the non-nitride spacer, thereby erasing a programmed cell in the non-volatile memory.